ABSTRACT

A double data rate (DDR) synchronous dynamic RAM (SDRAM), or DDR-SDRAM, memory controller employing a delay locked loop (DLL) circuit to delay an SDRAM data strobe (DQS) signal to the center, or 'eye' of the read data window. However, in distinction from conventional techniques, the initial delay determined by the DLL is fine tuned with an offset determined by a memory test. Moreover, in an additional embodiment, the delay may be further adjusted during operation to compensate for environmental conditions by a PVT (process, value, temperature) circuit.